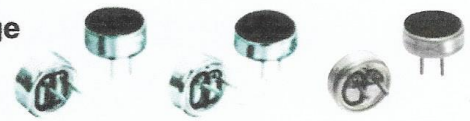
LAMPIRAN

Omnidirectional Back Electret Condenser Microphone Cartridge



Series: **WM-62PC/62PK** (pin type)
WM-64PC/64PK (pin type)
WM-64PN (pin type)

■ Features

- Provides special lead pins which realize connector connection or direct-in to PCB
- Very small, thin type omnidirectional microphone
- Most suited to products having limited space
- Back electret type designed for high resistance to vibrations
- Better shielded, RF noise-resistant type

■ Recommended Applications

- WM-62PC/64PC (33 pF)—GSM, PDC, etc.
- WM-62PK/64PK (10 pF)—DECT, PHS, PCN, PCS, etc.
- WM-64PN (33pF,10pF)—Dual Band

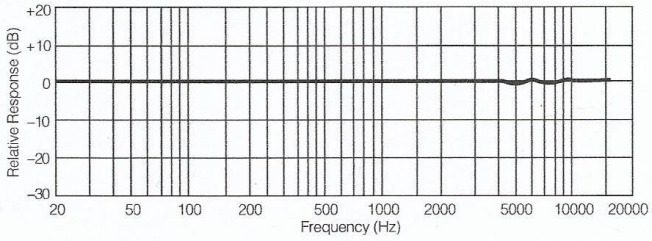
■ Sensitivity

	WM-62PC/62PK	WM-64PC/64PK/64PN
Vs = 2.0V RL = 2.2kΩ	–45 ± 4dB (X: –46 ± 3dB T: –44 ± 3dB U: –40 ± 3dB)	–45 ± 4dB (X: –46 ± 3dB T: –44 ± 3dB)

■ Specifications

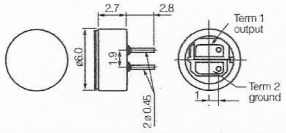
Sensitivity	–45±4dB (0dB = 1V/Pa, 1kHz)
Impedance	Less than 2.2 kΩ
Directivity	Omnidirectional
Frequency	20–16,000 Hz
Max. operation voltage	10V
Standard operation voltage	2V
Current consumption	Max. 0.5 mA
Sensitivity reduction	Within –3 dB at 1.5V
S/N ratio	More than 58 dB

■ Typical Frequency Response Curve

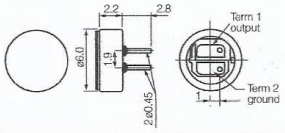


■ Dimensions in mm (not to scale)

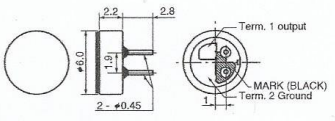
WM-62PC/62PK



WM-64PC/64PK



WM-64PN



Features

- High-performance, Low-power Atmel AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers + Peripheral Control Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 64 Kbytes of In-System Reprogrammable Flash program memory
  - 2 Kbytes EEPROM
  - 4 Kbytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[1]
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - Up to 64 Kbytes Optional External Memory Space
  - Programming Lock for Software Security
  - SPI Interface for In-System Programming
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - Two Expanded 16-bit Timer/Counters with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Two 8-bit PWM Channels
  - 6 PWM Channels with Programmable Resolution from 1 to 16 Bits
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels
    2 Differential Channels with Programmable Gain (1x, 10x, 200x)
  - Byte-oriented Two-wire Serial Interface
  - Dual Programmable Serial USARTs
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
  - Software Selectable Clock Frequency
  - ATmega103 Compatibility Mode Selected by a Fuse
  - Global Pull-up Disable
- I/O and Packages
  - 53 Programmable I/O Lines
  - 64-lead TQFP and 64-pad QFN/MLF
- Operating Voltages
  - 2.7V - 5.5V for Atmel ATmega64L
  - 4.5V - 5.5V for Atmel ATmega64
- Speed Grades
  - 0 - 8 MHz for ATmega64L
  - 0 - 16 MHz for ATmega64

Atmel

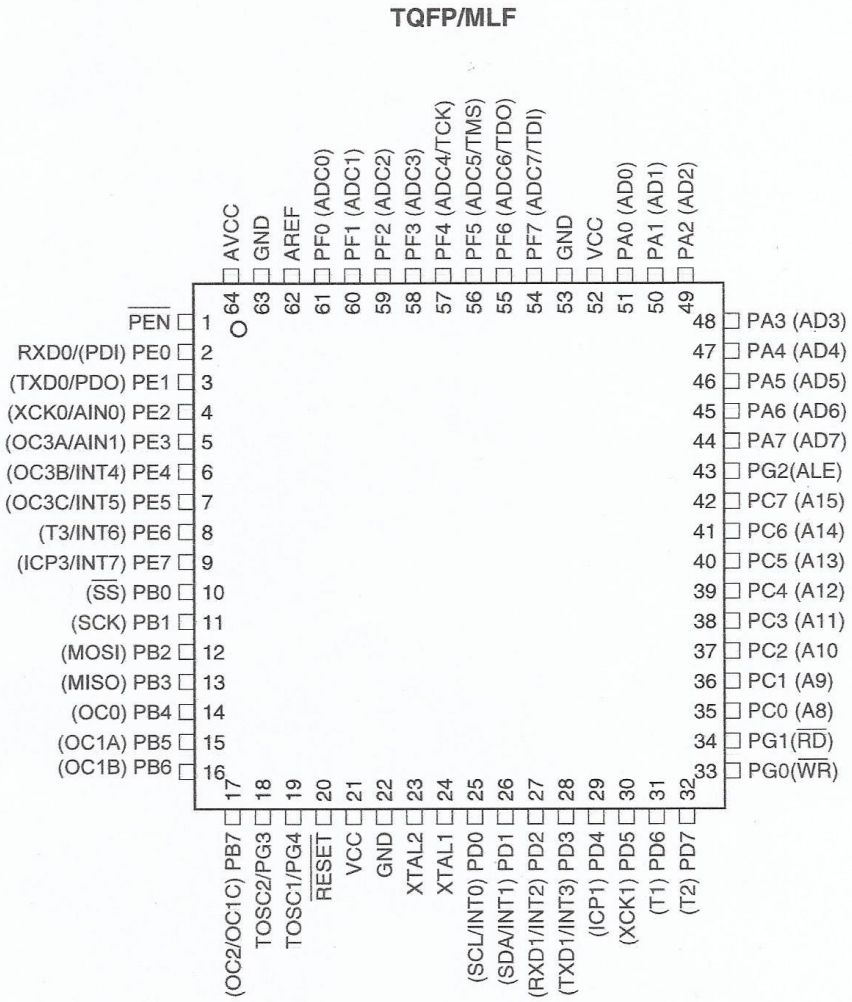
8-bit Atmel Microcontroller with 64K Bytes In-System Programmable Flash

ATmega64
ATmega64L

2490R–AVR–02/2013

Pin Configuration

Figure 1. Pinout ATmega64



Note: The bottom pad under the QFN/MLF package should be soldered to ground.

Disclaimer

Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

External Interrupts

The External Interrupts are triggered by the INT7:0 pins. Observe that, if enabled, the interrupts will trigger even if the INT7:0 pins are configured as outputs. This feature provides a way of generating a software interrupt. The external interrupts can be triggered by a falling or rising edge or a low level. This is set up as indicated in the specification for the External Interrupt Control Registers – EICRA (INT3:0) and EICRB (INT7:4). When the External Interrupt is enabled and is configured as level triggered, the interrupt will trigger as long as the pin is held low. Note that recognition of falling or rising edge interrupts on INT7:4 requires the presence of an I/O clock, described in "Clock Systems and their Distribution" on page 37. Low level interrupts and the edge interrupt on INT3:0 are detected asynchronously. This implies that these interrupts can be used for waking the part also from sleep modes other than Idle mode. The I/O clock is halted in all sleep modes except Idle mode.

Note that if a level triggered interrupt is used for wake-up from Power-down mode, the changed level must be held for some time to wake up the MCU. This makes the MCU less sensitive to noise. The changed level is sampled twice by the Watchdog Oscillator clock. The period of the Watchdog Oscillator is 1 µs (nominal) at 5.0V and 25°C. The frequency of the Watchdog Oscillator is voltage dependent as shown in the "Electrical Characteristics – TA = -40°C to 85°C" on page 325. The MCU will wake up if the input has the required level during this sampling or if it is held until the end of the start-up time. The start-up time is defined by the SUT Fuses as described in "Clock Systems and their Distribution" on page 37. If the level is sampled twice by the Watchdog Oscillator clock but disappears before the end of the start-up time, the MCU will still wake up, but no interrupt will be generated. The required level must be held long enough for the MCU to complete the wake up to trigger the level interrupt.

EICRA – External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0	
(0x6A)	ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00	EICRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

This Register can not be reached in ATmega103 compatibility mode, but the Initial Value defines INT3:0 as low level interrupts, as in ATmega103.

- **Bits 7..0 – ISC31, ISC30 - ISC00, ISC00: External Interrupt 3 - 0 Sense Control Bits**

The External Interrupts 3 - 0 are activated by the external pins INT3:0 if the SREG I-flag and the corresponding interrupt mask in the EIMSK is set. The level and edges on the external pins that activate the interrupts are defined in Table 48. Edges on INT3..INT0 are registered asynchronously. Pulses on INT3:0 pins wider than the minimum pulse width given in Table 49 will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt. If enabled, a level triggered interrupt will generate an interrupt request as long as the pin is held low. When changing the ISCn bit, an interrupt can occur. Therefore, it is recommended to first disable INTn by clearing its Interrupt Enable bit in the EIMSK Register. Then, the ISCn bit can be changed. Finally, the INTn interrupt flag should be cleared by writing a logical one to its Interrupt Flag bit (INTFn) in the EIFR Register before the interrupt is re-enabled.